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<b>UTILITY PATENT APPLICATION TRANSMITTAL</b> (Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))	Attorney Docket No.	MI22-1398
	First Inventor or Application Identifier	Weimin Li et al.
	Title	Low k Interlevel Dielectric Layer Fabrication Methods
	Express Mail Label No.	EL 465682468 US

<b>APPLICATION ELEMENTS</b> See MPEP chapter 600 concerning utility patent application contents.		<b>ADDRESS TO:</b> Assistant Commissioner for Patents Box Patent Application Washington, DC 20231			
1. <input checked="" type="checkbox"/> * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing)	5. <input type="checkbox"/> Microfiche Computer Program (Appendix)	JCS596 U.S. PTO 09/536037 03/27/00			
2. <input checked="" type="checkbox"/> Specification [Total Pages 30] 1 (preferred arrangement set forth below) - Descriptive title of the Invention <u>PLUS TITLE PAGE</u> - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure	6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary) a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies				
3. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) [Total Sheets 1] 1	<b>ACCOMPANYING APPLICATION PARTS</b>				
4. Oath or Declaration [Total Pages 2] 1 a. <input type="checkbox"/> Newly executed (original or copy) b. <input checked="" type="checkbox"/> Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 16 completed) i. <input type="checkbox"/> <u>DELETION OF INVENTOR(S)</u> Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).	7. <input type="checkbox"/> Assignment Papers (cover sheet & document(s)) 8. <input type="checkbox"/> 37 C.F.R. § 3.73(b) Statement <input type="checkbox"/> Power of Attorney (when there is an assignee) 9. <input type="checkbox"/> English Translation Document (if applicable) 10. <input checked="" type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations 11. <input checked="" type="checkbox"/> Preliminary Amendment 12. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) (Should be specifically itemized) 13. <input type="checkbox"/> * Small Entity Statement(s) <input type="checkbox"/> Statement filed in prior application (PTO/SB/09-12) Status still proper and desired 14. <input type="checkbox"/> Certified Copy of Priority Document(s) (if foreign priority is claimed) 15. <input checked="" type="checkbox"/> Other: <u>Check for \$708</u>				
<b>NOTE FOR ITEMS 1 &amp; 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).</b>					

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No: 09/388,826  
Prior application information: Examiner M. Whipple Group / Art Unit: 2812

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

**17. CORRESPONDENCE ADDRESS**

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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. .... 09/388,826  
Priority Filing Date ..... September 1, 1999  
Inventor ..... Weimin Li et al.  
Assignee ..... Micron Technology, Inc.  
Priority Group Art Unit ..... 2812  
Priority Examiner ..... M. Whipple  
Attorney's Docket No. .... MI22-1398  
Title: Low k Interlevel Dielectric Layer Fabrication Methods

PRELIMINARY AMENDMENT

To: Assistant Commissioner for Patents  
Washington, D.C. 20231

From: Mark S. Matkin (Tel. 509-624-4276; Fax 509-838-3424)  
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Sir:

Please enter the following amendments prior to examining the  
above-identified application. Applicant amends and remarks as follows:  
[unless otherwise indicated, deletions are bracketed, additions are  
underlined].

AMENDMENTSIn the Specification

At p. 2, line 15, replace "a exemplary" with --an exemplary--.

1     **--RELATED PATENT DATA**

2             This patent application is a divisional resulting from U.S.  
3     Patent Application Serial No. 09/388,826, filed September 1, 1999,  
4     entitled "Low k Interlevel Dielectric Layer Fabrication Methods",  
5     naming Weimin Li, Zhiping Yin, and William Budge as inventors,  
6     and which is now U.S. Patent No. \_\_\_\_\_, the  
7     disclosure of which is incorporated by reference.--

8  
9     **Amended Claims**


10            Please cancel claims 1-25 and 34-51.  
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REMARKS

Claims 1-25 and 34-51 are cancelled. Claims 26-33 and 52-64 are in the application for consideration.

Respectfully submitted,

Dated: 3-27-00

By:   
Mark S. Matkin  
Reg. No. 32,268

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EL 465682468

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

\* \* \* \* \*

Low k Interlevel Dielectric Layer Fabrication  
Methods

\* \* \* \* \*

INVENTORS

Weimin Li  
Zhiping Yin  
William Budge

ATTORNEY'S DOCKET NO. MI22-1208

# Low k Interlevel Dielectric Layer Fabrication Methods

## TECHNICAL FIELD

This invention relates to methods of forming low k interlevel dielectric layers.

## BACKGROUND OF THE INVENTION

In methods of forming integrated circuits, it is frequently desired to electrically isolate components of the integrated circuits from one another with an insulative material. For example, conductive layers can be electrically isolated from one another by separating them with an insulating material. Insulating material received between two different elevation conductive or component layers is typically referred to as an interlevel dielectric material. Also, devices which extend into a semiconductive substrate can be electrically isolated from one another by insulative materials formed within the substrate between the components, such as for example, trench isolation regions.

One typical insulative material for isolating components of integrated circuits is silicon dioxide, which has a dielectric constant of about 4. Yet in many applications, it is desired to utilize insulative materials having dielectric constants lower than that of silicon dioxide to reduce parasitic capacitance from occurring between conductive components separated by the insulative material. Parasitic capacitance

1 reduction continues to have increasing importance in the semiconductor  
2 fabrication industry as device dimensions and component spacing  
3 continues to shrink. Closer spacing adversely effects parasitic  
4 capacitance.

5 One way of reducing the dielectric constant of certain inherently  
6 insulative materials is to provide some degree of carbon content therein.  
7 One example technique for doing so has recently been developed by  
8 Trikon Technology of Bristol, UK which they refer to as Flowfill<sup>tm</sup>  
9 Technology. Where more carbon incorporation is desired, methylsilane  
10 in a gaseous form and  $H_2O_2$  in a liquid form are separately introduced  
11 into a chamber, such as a parallel plate reaction chamber. A reaction  
12 between the methylsilane and  $H_2O_2$  can be moderated by introduction  
13 of nitrogen into the reaction chamber. A wafer is provided within the  
14 chamber and ideally maintained at a suitable low temperature, such as  
15  $0^\circ C$ , at a exemplary pressure of 1 Torr to achieve formation of a  
16 methylsilanol structure. Such structure/material condenses on the wafer  
17 surface. Although the reaction occurs in the gas phase, the deposited  
18 material is in the form of a viscus liquid which flows to fill small gaps  
19 on the wafer surface. In applications where deposition thickness  
20 increases, surface tension drives the deposited layer flat, thus forming  
21 a planarized layer over the substrate.

22 The liquid methylsilanol is converted to a silicon dioxide structure  
23 by a two-step process occurring in two separate chambers from that in  
24 which the silanol-type structure was deposited. First, planarization of

1 the liquid film is promoted by increasing the temperature to above 100°  
2 C, while maintaining the pressure at about 1 Torr, to result in  
3 solidification and formation of a polymer layer. Thereafter, the  
4 temperature is raised to approximately 450°C, while maintaining a  
5 pressure of about 1 Torr, to form  $(\text{CH}_3)_x\text{SiO}_y$ . The  $(\text{CH}_3)_x\text{SiO}_y$  has  
6 a dielectric constant of less than or equal to about 3, and is  
7 accordingly less likely to be involved in parasitic capacitance than silicon  
8 dioxide and/or phosphorous doped silicon dioxide.

9 Nevertheless, it would be desirable to develop improved methods  
10 for reducing parasitic capacitance of interlevel dielectric layers which  
11 comprise carbon and regardless of the method of manufacture of such  
12 layers.

### 13 SUMMARY

14  
15  
16 The invention comprises methods of forming low k interlevel  
17 dielectric layers. In one implementation, a low k interlevel dielectric  
18 layer fabrication method includes providing a substrate having integrated  
19 circuitry at least partially formed thereon. An oxide comprising  
20 interlevel dielectric layer comprising carbon and having a dielectric  
21 constant no greater than 3.5 is formed over the substrate. After  
22 forming the carbon comprising dielectric layer, it is exposed to a plasma  
23 comprising oxygen effective to reduce the dielectric constant to below  
24 what it was prior to said exposing.



1 In one implementation, a low k interlevel dielectric layer  
2 fabrication method includes providing a substrate having integrated  
3 circuitry at least partially formed thereon. In a chamber, an interlevel  
4 dielectric layer comprising carbon and having a dielectric constant no  
5 greater than 3.5 is plasma enhanced chemical vapor deposited over the  
6 substrate at subatmospheric pressure. After forming the carbon  
7 comprising dielectric layer, it is exposed to a plasma comprising oxygen  
8 at a subatmospheric pressure effective to reduce the dielectric constant  
9 by at least 10% below what it was prior to said exposing. The  
10 exposing occurs without removing the substrate from the chamber  
11 between the depositing and the exposing, and pressure within the  
12 chamber is maintained at subatmospheric between the depositing and the  
13 exposing.

14 In one implementation, a low k interlevel dielectric layer  
15 fabrication method includes providing a substrate having integrated  
16 circuitry at least partially formed thereon. An interlevel dielectric layer  
17 comprising a compound having silicon bonded to both nitrogen and an  
18 organic material and having a dielectric constant no greater than 8.0  
19 over is formed over the substrate. After forming the dielectric layer,  
20 it is exposed to a plasma comprising nitrogen effective to reduce the  
21 dielectric constant to below what it was prior to said exposing.  
22  
23  
24

## BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer at a processing step subsequent to that shown by Fig. 1.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, an exemplary semiconductor wafer fragment or substrate in process is indicated generally with reference numeral 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

1 Substrate 10 comprises a bulk monocrystalline silicon substrate 12  
2 having trench isolation oxide regions 14 formed therein. Integrated  
3 circuitry is at least partially formed thereon in the illustrated example  
4 in the form of a pair of transistors 16 and 18. Transistors 16 and 18  
5 can comprise conventional constructions, such as overlying layers of gate  
6 oxide, polysilicon and silicide. Insulative spacers 20 are formed adjacent  
7 transistor gates 16 and 18. Conductively doped diffusion regions 22, 24  
8 and 26 are formed within substrate 12 and proximate gates 16 and 18.

9 Referring to Fig. 2 and in accordance with but one aspect of the  
10 invention, an interlevel dielectric layer 30 comprising carbon and having  
11 a dielectric constant no greater than 3.5 is formed over the Fig. 1  
12 substrate where layer 30 comprises oxide material. Such layer might be  
13 formed by a number of methods. One example preferred method  
14 includes the Flowfill<sup>tm</sup> technique referred to above, whereby the formed  
15 interlevel dielectric level comprises or ultimately consists essentially of  
16  $(CH_3)_xSiO_y$ , where x ranges from 1 to 3, and y ranges from 0-2. Such  
17 provides but one example where the dielectric layer formed comprises  
18 silicon bonded to organic material. Other dielectric layers, as well as  
19 the same or other layers, fabricated by different methods are also  
20 contemplated.

21 By way of example only, example preferred alternate methods of  
22 producing an interlevel dielectric layer at this point in the process are  
23 now described. Such encompass methods of forming insulative materials  
24 comprising carbon, silicon and oxygen. In one example, a first gaseous

precursor compound comprising carbon and silicon is combined with a second gaseous precursor compound comprising oxygen to form a second compound comprising carbon, silicon and oxygen. The first compound can comprise, for example,  $(\text{CH}_3)_y\text{SiH}_x$ , wherein y is an integer of from 1 to 4 and x is an integer from 0 to 3. The second precursor compound is an oxygen-containing moiety that is preferably a "dry" compound (i.e., a compound that does not either contain water or decompose to form water), and can comprise, for example,  $\text{N}_2\text{O}$ , or an activated oxygen species (e.g., high energy  $\text{O}_2$ , monatomic oxygen, or oxygen radicals). Such provides but one example process whereby water formation is avoided. In one example, the oxygen-containing moiety is generated by exposing  $\text{O}_2$  to ultra-violet light (a process which can generate, for example, activated oxygen species in the form of  $\text{O}_3$ ). In another aspect, the oxygen-containing moiety is generated by exposing an oxygen-containing gas (e.g.,  $\text{O}_3$ ,  $\text{O}_2$ ,  $\text{N}_2\text{O}$ ,  $\text{CO}$ , or  $\text{CO}_2$ ) to a plasma. The plasma can be within the reaction chamber or remote from the chamber (i.e., not in the chamber). In another example, a compound comprising silicon, carbon and oxygen is formed by reaction of  $\text{SiH}_4$  with an organic compound comprising oxygen (e.g.,  $\text{CO}$  or  $\text{CO}_2$ ).

In a more specific example, methylsilane or trimethylsilane is combined with  $\text{N}_2\text{O}$  in a reaction chamber. A pressure within the chamber is maintained at from about 300 mTorr to about 30 Torr, and is preferably maintained at from about 1 Torr to about 10 Torr. An

1 exemplary reaction chamber comprises a spacing from about 400 mils  
2 to about 600 mils with methylsilane being flowed into the chamber at  
3 a rate from about 25 standard cubic centimeters per minute (sccm) to  
4 about 2000 sccm (preferably at from about 50 sccm to about 250 sccm).  
5 The N<sub>2</sub>O is flowed into the reaction chamber at a rate from about 50  
6 sccm to about 3000 sccm (preferably at a rate from about 100 sccm to  
7 about 1500 sccm, and more preferably at a rate of from about 500  
8 sccm to about 1200 sccm), and, additionally, helium is flowed into the  
9 reaction chamber at a rate of about 500 sccm to about 5000 sccm  
10 (preferably from 1000 sccm to about 3000 sccm). A radio frequency  
11 (RF) power within the chamber is maintained at from about 50 watts  
12 to about 500 watts, and preferably from about 100 watts to about 200  
13 watts. The semiconductor substrate (such as a monocrystalline silicon  
14 wafer) is provided within the chamber and maintained at a temperature  
15 from about 25°C to about 450°C.

16 The above-described processing forms (CH<sub>3</sub>)<sub>x</sub>SiO<sub>y</sub> over a substrate.  
17 The concentration of methyl groups within the (CH<sub>3</sub>)<sub>x</sub>SiO<sub>y</sub> is typically  
18 from about 10% to about 50% (mole percent), i.e., where x equals or  
19 ranges from about 1 to about 3, and y ranges from 0 to about 2.  
20 Alternately by way of example only, x can be from about 0.1 to about  
21 1, i.e., the concentration of methyl groups can be from about 5% to  
22 about 50% molar. In a particular example, a plasma can be generated  
23 within the chamber at a RF power of from about 50 watts to about  
24 500 watts (preferably from about 80 watts to about 200 watts).

Such describes but one example process of forming an interlevel dielectric layer, here by chemical vapor deposition with or without plasma in a chemical vapor deposition chamber. In but another considered example, a gaseous precursor compound is introduced into a chemical vapor deposition reaction chamber and subjected to a plasma treatment. A semiconductor substrate is provided in the chamber, and material comprising carbon and silicon is deposited from the plasma-treated precursor compound to over the substrate. After the material is deposited, it is exposed to an oxygen containing moiety and converted to a second material comprising silicon, carbon and oxygen.

In a more specific example, methylsilane is flowed into a reaction chamber at a pressure of from 300 mTorr to about 30 Torr (preferably from about 1 Torr to about 10 Torr) and subjected to a plasma formed at a power of from about 50 watts to about 500 watts (preferably from 100 watts to about 200 watts). A semiconductor substrate is provided in the reaction chamber and maintained at a temperature of about 0° C to about 600° C. The plasma treated methylsilane deposits a material comprising methyl groups and silicon over the substrate. The deposited material is then exposed to an oxygen-containing moiety to convert the material to  $(CH_3)_xSiO_y$ . Accordingly in this example from the oxygen exposure, a whole of the deposited dielectric layer is transformed from one base chemistry (i.e., that comprising a nondescript combination of methyl groups and silicon) to another base chemistry (i.e.,  $(CH_3)_xSiO_y$ ) by the oxygen exposure. The oxygen-containing

1 moiety is preferably in gaseous form, and can comprise, for example  
2 ozone,  $O_2$  and/or  $N_2O$ . In particular embodiments, the oxygen-  
3 containing moiety is subjected to plasma, heat or ultra-violet light. The  
4 oxygen treatment preferably occurs at a pressure of from about 300  
5 mTorr to about 1 atmosphere, with the deposited material being  
6 maintained at a temperature of from about  $0^\circ C$  to about  $600^\circ C$  during  
7 the oxygen treatment to convert the base chemistry to  $(CH_3)_xSiO_y$ .

8 The above-described processings are again only example preferred  
9 techniques of forming the preferred interlevel dielectric layer material  
10 comprising carbon, here in the form of  $CH_3$ , and here producing a  
11 preferred layer of  $(CH_3)_xSiO_y$ . Alternate interlevel dielectric materials  
12 comprising carbon are of course contemplated. Further and by way of  
13 example only, the deposited interlevel dielectric layer at this point in  
14 the process might comprise silicon atoms bonded to both organic  
15 material and nitrogen, for example as described below.

16 After forming carbon comprising dielectric layer 30, in but one  
17 aspect of the invention, such layer is exposed to a plasma comprising  
18 oxygen effective to reduce the dielectric constant to below what it was  
19 prior to said exposing. Preferably, the exposing is at subatmospheric  
20 pressure to reduce the dielectric constant by at least 10%, and even  
21 more preferably by at least 15%, below what it was prior to said  
22 exposing. In a most preferred embodiment, the method by which the  
23 interlevel dielectric layer is initially formed is by plasma enhanced  
24 chemical vapor deposition in a chamber, with the subsequent exposing

1 of the plasma occurring in subatmospheric pressure in the same  
2 chamber. Further, the substrate is preferably not removed from the  
3 chamber between the depositing and the exposing. Further, the  
4 pressure within the chamber is preferably maintained at subatmospheric  
5 between the depositing and the exposing. Further, the exposing is  
6 ideally effective to increase stability of the dielectric constant to  
7 variation from what the stability was prior to the exposing. Specifically,  
8 stability of the dielectric constant of interlevel dielectric materials can  
9 have a tendency to increase over time or when exposed to subsequent  
10 thermal processing of at least 400°C. Ideally, the exposing is also  
11 effective to increase the stability of the dielectric constant of such film.

12 Exemplary processing in accordance with the invention has been  
13 achieved whereby a predominately  $(\text{CH}_3)_x\text{SiO}_y$  interlevel dielectric layer  
14 after the exposing had a dielectric constant reduced from 3.0 to about  
15 2.5 or 2.0.

16 The preferred wafer surface temperature during the exposing is  
17 always less than or equal to 550°C, with the exposing also preferably  
18 being conducted at subatmospheric pressure. The oxygen comprising  
19 plasma is preferably derived at least in part from at least one of  $\text{O}_2$ ,  
20  $\text{O}_3$ ,  $\text{N}_2\text{O}$ , and  $\text{NO}_x$ . Preferred parameters for the exposing in a dual  
21 plate capacitively coupled reactor include an RF power range of from  
22 300 to 1000 watts, a pressure range of from 1 Torr to 6 Torr, a  
23 temperature range of from 100°C to 450°C, a spacing between the  
24 plates of from 400 to 600 mils, an oxygen gas exposure flow of from



500 to 1500 sccm, an inert gas flow (i.e., He and/or Ar) of from 200 sccm to 800 sccm, and a treatment time of from 20 to 100 to more seconds. It is a preferred intent of the exposing to further not transform a whole of all of the dielectric layer from one base chemistry to another base chemistry by the exposing. An outermost portion of the exposed layer might experience a slight reduction in carbon content, but otherwise that portion and the whole of the layer is not transformed from one fundamental material to another even in spite of the low k reducing or resulting property. In one preferred aspect of the invention, the exposing comprises at least 20 seconds of processing time. More preferably and in preferred sequence, the processing comprises at least 40 seconds, 60 seconds, 80 seconds, and 100 seconds of oxygen containing plasma exposure. The plasma exposing is preferably ineffective to appreciably etch the interlevel dielectric layer.

Where the invention is conducted *in situ* in a plasma enhanced chemical vapor deposition chamber subsequent to the deposition, the exposing might comprise substantially ceasing feeding of one of the reactive gases while maintaining a feed of one of the precursors which comprises oxygen, and thereby maintaining plasma conditions from the deposition through an extended exposure time with the oxygen containing precursor to achieve the exposing effect.

In another considered aspect of the invention, a nitride comprising interlevel dielectric layer 30 is formed over the substrate to also comprise carbon and having a dielectric constant no greater than 8.0.

1 More preferred, interlevel dielectric layer 30 comprises a compound  
2 having silicon bonded to both nitrogen and an organic material and  
3 having a dielectric constant no greater than 8.0. After forming such  
4 dielectric layer, it is exposed to a plasma comprising nitrogen effective  
5 to reduce the dielectric constant to below what it was prior to said  
6 exposing, and preferably at least 15% below what it was prior to the  
7 exposing. By way of example only, a preferred deposited interlevel  
8 dielectric layer material comprises or consists essentially of  
9  $(\text{CH}_3)_x\text{Si}_3\text{N}_{(4-x)}$ , wherein x is greater than 0 and no greater than 4.  
10 Such a composition can be formed by, for example, reacting inorganic  
11 silane with one or more of ammonia ( $\text{NH}_3$ ), hydrazine ( $\text{N}_2\text{H}_4$ ), or a  
12 combination of nitrogen ( $\text{N}_2$ ) and hydrogen ( $\text{H}_2$ ). The reaction can  
13 occur with or without plasma. However, if the reaction comprises an  
14 organic silane in combination with dinitrogen and dihydrogen, the  
15 reaction preferably occurs in the presence of plasma.

16 An exemplary specific reaction is to combine methylsilane  
17  $(\text{CH}_3\text{SiH}_3)$  with  $\text{NH}_3$  in the presence of a plasma to form  
18  $(\text{CH}_3)_x\text{Si}_3\text{N}_{(4-x)}$ . The exemplary reaction can occur, for example, under  
19 the following conditions. A substrate is placed within a reaction  
20 chamber of a reactor, and a surface of the substrate is maintained at  
21 a temperature of from about  $0^\circ\text{C}$  to about  $600^\circ\text{C}$ . Ammonia and  
22 methyl silane are flowed into the reaction chamber, and a pressure  
23 within the chamber is maintained at from about 300 mTorr to about  
24 30 Torr, with a plasma at a radio frequency (RF) power of from about

50 watts to about 500 watts. A product comprising  $(\text{CH}_3)_x\text{Si}_3\text{N}_{(4-x)}$  is then formed and deposited on the substrate.

Using this particular described example, it was found that the product deposited from the described reaction consists essentially of  $(\text{CH}_3)_x\text{Si}_3\text{N}_{(4-x)}$ , (wherein x is generally about 1). The  $(\text{CH}_3)_x\text{Si}_3\text{N}_{(4-x)}$  is present in the product to a concentration of from greater than 0% to about 50% (mole percent) and is preferably from about 10% to about 20%. The amount of  $(\text{CH}_3)_x\text{Si}_3\text{N}_{(4-x)}$  present in the product can be adjusted by providing a feed gas of  $\text{SiH}_4$  in the reactor in addition to the  $\text{CH}_3\text{SiH}_3$ , and by varying a ratio of the  $\text{SiH}_4$  to the  $\text{CH}_3\text{SiH}_3$ , and/or by adjusting RF power.

The above provides but only one example of forming an interlevel dielectric layer comprising a compound having silicon bonded to both nitrogen and an organic material. Other methods of forming the same or different materials are of course contemplated.

After forming the dielectric layer, the nitrogen comprising plasma to which the layer is exposed preferably comprises one or more of  $\text{N}_2$ ,  $\text{NH}_3$ ,  $\text{N}_2\text{H}_4$ ,  $\text{N}_2\text{O}$ , and  $\text{NO}_x$ . More preferably, the plasma exposing is preferably void of oxygen atoms therein. Wherein the dielectric layer is formed by chemical vapor deposition in a chamber, such as described above, the exposing preferably occurs within the chamber without removing the substrate from the chamber between the forming and the exposing. Again, the plasma exposing like in the first described

1 example is preferably conducted to be ineffective to appreciably etch the  
2 interlevel dielectric layer. Further, a whole of the dielectric layer  
3 subjected to the exposing is preferably not transformed from one base  
4 chemistry to another by the exposing. Preferred temperature, pressure,  
5 power, space arrangements, flows, and treatment times are as described  
6 above with respect to the first described embodiments.

7 In compliance with the statute, the invention has been described  
8 in language more or less specific as to structural and methodical  
9 features. It is to be understood, however, that the invention is not  
10 limited to the specific features shown and described, since the means  
11 herein disclosed comprise preferred forms of putting the invention into  
12 effect. The invention is, therefore, claimed in any of its forms or  
13 modifications within the proper scope of the appended claims  
14 appropriately interpreted in accordance with the doctrine of equivalents.  
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1     CLAIMS:

2           1.     A low k interlevel dielectric layer fabrication method  
3     comprising:

4           providing a substrate having integrated circuitry at least partially  
5     formed thereon;

6           forming an oxide comprising interlevel dielectric layer comprising  
7     carbon and having a dielectric constant no greater than 3.5 over said  
8     substrate; and

9           after forming the carbon comprising dielectric layer, exposing it to  
10    a plasma comprising oxygen effective to reduce the dielectric constant  
11    to below what it was prior to said exposing.

12  
13           2.     The method of claim 1 wherein the exposing is effective to  
14    increase stability of the dielectric constant to variation from what it was  
15    prior to the exposing.

16  
17           3.     The method of claim 1 comprising exposing the carbon  
18    comprising dielectric layer to a plasma comprising oxygen effective to  
19    reduce the dielectric constant to at least 15% below what it was prior  
20    to said exposing.

21  
22           4.     The method of claim 1 wherein the oxygen comprising  
23    plasma is at least in part derived from O<sub>2</sub>.  
24

1           5.    The method of claim 1 wherein the oxygen comprising  
2 plasma is at least in part derived from  $O_3$ .

3  
4           6.    The method of claim 1 wherein the oxygen comprising  
5 plasma is at least in part derived from  $N_2O$ .

6  
7           7.    The method of claim 1 wherein the oxygen comprising  
8 plasma is at least in part derived from  $NO_x$ .

9  
10          8.    The method of claim 1 wherein the dielectric layer  
11 comprising carbon is formed by chemical vapor deposition in a chamber,  
12 the exposing occurring within the chamber without removing the  
13 substrate from the chamber between the forming and the exposing.

14  
15          9.    The method of claim 8 wherein the chemical vapor  
16 deposition is plasma enhanced.

17  
18          10.   The method of claim 1 wherein the temperature during the  
19 exposing is always less than or equal to  $550^{\circ}C$ .

20  
21          11.   The method of claim 1 wherein the plasma exposing is  
22 ineffective to appreciably etch the interlevel dielectric layer.

12. The method of claim 1 wherein the dielectric layer subjected to the exposing comprises silicon bonded to organic material.

13. The method of claim 1 wherein the dielectric layer subjected to the exposing comprises silicon atoms bonded to both organic material and nitrogen.

14. The method of claim 1 wherein the carbon is present as a  $\text{CH}_3$  group.

15. The method of claim 1 wherein the dielectric layer subjected to the exposing comprises  $(\text{CH}_3)_x\text{SiO}_y$ .

16. The method of claim 1 wherein the dielectric layer subjected to the exposing comprises  $(\text{CH}_3)_x\text{SiO}_y$  which remains as  $(\text{CH}_3)_x\text{SiO}_y$  after the exposing.

17. The method of claim 1 wherein the dielectric layer subjected to the exposing consists essentially of  $(\text{CH}_3)_x\text{SiO}_y$ .

1           18. The method of claim 1 wherein the dielectric layer subjected  
2 to the exposing comprises  $(\text{CH}_3)_x\text{SiO}_y$  which remains as  $(\text{CH}_3)_x\text{SiO}_y$   
3 after the exposing, and wherein the exposing comprises at least 20  
4 seconds.

5  
6           19. The method of claim 1 wherein a whole of the dielectric  
7 layer subjected to the exposing is not transformed from one base  
8 chemistry to another by the exposing.

9  
10          20. The method of claim 1 wherein the dielectric layer subjected  
11 to the exposing comprises silicon bonded to organic material, a whole  
12 of the dielectric layer subjected to the exposing is not transformed from  
13 one base chemistry to another by the exposing, and the exposing  
14 comprises at least 20 seconds.

15  
16          21. The method of claim 1 wherein the dielectric layer subjected  
17 to the exposing comprises silicon bonded to organic material, a whole  
18 of the dielectric layer subjected to the exposing is not transformed from  
19 one base chemistry to another by the exposing, and the exposing  
20 comprises at least 40 seconds.



1           22. The method of claim 1 wherein the dielectric layer subjected  
2 to the exposing comprises silicon bonded to organic material, a whole  
3 of the dielectric layer subjected to the exposing is not transformed from  
4 one base chemistry to another by the exposing, and the exposing  
5 comprises at least 60 seconds.  
6

7           23. The method of claim 1 wherein the dielectric layer subjected  
8 to the exposing comprises silicon bonded to organic material, a whole  
9 of the dielectric layer subjected to the exposing is not transformed from  
10 one base chemistry to another by the exposing, and the exposing  
11 comprises at least 80 seconds.  
12

13           24. The method of claim 1 wherein the dielectric layer subjected  
14 to the exposing comprises silicon bonded to organic material, a whole  
15 of the dielectric layer subjected to the exposing is not transformed from  
16 one base chemistry to another by the exposing, and the exposing  
17 comprises at least 100 seconds.  
18

19           25. The method of claim 1 wherein the majority of the carbon  
20 present in the dielectric layer is in the form of methyl groups, and  
21 wherein the methyl groups comprise from 10% to about 50% of the  
22 dielectric layer (mole percent) before and after the exposing.  
23  
24

1           26. A low k interlevel dielectric layer fabrication method  
2 comprising:

3           providing a substrate having integrated circuitry at least partially  
4 formed thereon;

5           forming a nitride comprising interlevel dielectric layer comprising  
6 carbon and having a dielectric constant no greater than 8.0 over said  
7 substrate; and

8           after forming the carbon comprising dielectric layer, exposing it to  
9 a plasma comprising nitrogen effective to reduce the dielectric constant  
10 to below what it was prior to said exposing.

11  
12           27. The method of claim 26 wherein the nitrogen comprising  
13 plasma is at least in part derived from  $N_2$ .

14  
15           28. The method of claim 26 wherein the nitrogen comprising  
16 plasma is at least in part derived from  $NH_3$ .

17  
18           29. The method of claim 26 wherein the nitrogen comprising  
19 plasma is at least in part derived from  $N_2H_4$ .

20  
21           30. The method of claim 26 wherein the nitrogen comprising  
22 plasma is at least in part derived from  $N_2O$ .

1           31. The method of claim 26 wherein the nitrogen comprising  
2 plasma is at least in part derived from NO<sub>x</sub>.

3  
4           32. The method of claim 26 wherein the dielectric layer  
5 comprising carbon is formed by chemical vapor deposition in a chamber,  
6 the exposing occurring within the chamber without removing the  
7 substrate from the chamber between the forming and the exposing.

8  
9           33. The method of claim 26 wherein the carbon is present as  
10 a CH<sub>3</sub> group.  
11  
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1           34. A low k interlevel dielectric layer fabrication method  
2 comprising:

3           providing a substrate having integrated circuitry at least partially  
4 formed thereon;

5           in a chamber, plasma enhanced chemical vapor depositing an  
6 interlevel dielectric layer comprising carbon and having a dielectric  
7 constant no greater than 3.5 over said substrate at subatmospheric  
8 pressure; and

9           after forming the carbon comprising dielectric layer, exposing it to  
10 a plasma comprising oxygen at a subatmospheric pressure effective to  
11 reduce the dielectric constant by at least 10% below what it was prior  
12 to said exposing, the exposing occurring without removing the substrate  
13 from the chamber between the depositing and the exposing, and  
14 pressure within the chamber being maintained at subatmospheric between  
15 the depositing and the exposing.

16  
17           35. The method of claim 34 wherein at least two precursors are  
18 fed to the chamber during the depositing, one of the precursors  
19 comprising oxygen, the exposing comprising substantially ceasing feeding  
20 another of the precursors while feeding the one, and maintaining plasma  
21 conditions within the chamber from the depositing through the exposing.  
22  
23  
24

1           36. The method of claim 34 wherein the plasma enhanced  
2 chemical vapor depositing comprises feeding a methyl silane to the  
3 chamber.

4  
5           37. The method of claim 34 wherein the dielectric layer  
6 comprises silicon bonded to organic material.

7  
8           38. The method of claim 34 wherein the dielectric layer  
9 comprises silicon atoms bonded to both organic material and nitrogen.

10  
11           39. The method of claim 34 wherein the oxygen comprising  
12 plasma is at least in part derived from  $O_2$ .

13  
14           40. The method of claim 34 wherein the oxygen comprising  
15 plasma is at least in part derived from  $O_3$ .

16  
17           41. The method of claim 34 wherein the oxygen comprising  
18 plasma is at least in part derived from  $N_2O$ .

19  
20           42. The method of claim 34 wherein the oxygen comprising  
21 plasma is at least in part derived from  $NO_x$ .

1           43. The method of claim 34 wherein the dielectric layer  
2 subjected to the exposing comprises  $(\text{CH}_3)_x\text{SiO}_y$ .

3  
4           44. The method of claim 34 wherein the dielectric layer  
5 subjected to the exposing comprises  $(\text{CH}_3)_x\text{SiO}_y$  which remains as  
6  $(\text{CH}_3)_x\text{SiO}_y$  after the exposing.

7  
8           45. The method of claim 34 wherein the dielectric layer  
9 subjected to the exposing consists essentially of  $(\text{CH}_3)_x\text{SiO}_y$ .

10  
11           46. The method of claim 34 wherein the dielectric layer  
12 subjected to the exposing comprises  $(\text{CH}_3)_x\text{SiO}_y$  which remains as  
13  $(\text{CH}_3)_x\text{SiO}_y$  after the exposing, and wherein the exposing comprises at  
14 least 20 seconds.

15  
16           47. The method of claim 34 wherein a whole of the dielectric  
17 layer subjected to the exposing is not transformed from one base  
18 chemistry to another by the exposing.

1           48. The method of claim 34 wherein the dielectric layer  
2 subjected to the exposing comprises silicon bonded to organic material,  
3 a whole of the dielectric layer subjected to the exposing is not  
4 transformed from one base chemistry to another by the exposing, and  
5 the exposing comprises at least 20 seconds.  
6

7           49. The method of claim 34 wherein the dielectric layer  
8 subjected to the exposing comprises silicon bonded to organic material,  
9 a whole of the dielectric layer subjected to the exposing is not  
10 transformed from one base chemistry to another by the exposing, and  
11 the exposing comprises at least 40 seconds.  
12

13           50. The method of claim 34 wherein the dielectric layer  
14 subjected to the exposing comprises silicon bonded to organic material,  
15 a whole of the dielectric layer subjected to the exposing is not  
16 transformed from one base chemistry to another by the exposing, and  
17 the exposing comprises at least 60 seconds.  
18

19           51. The method of claim 34 wherein the majority of the carbon  
20 present in the dielectric layer is in the form of methyl groups, and  
21 wherein the methyl groups comprise from 10% to about 50% of the  
22 dielectric layer (mole percent) before and after the exposing.  
23  
24

1           52. A low k interlevel dielectric layer fabrication method  
2 comprising:

3           providing a substrate having integrated circuitry at least partially  
4 formed thereon;

5           forming an interlevel dielectric layer comprising a compound having  
6 silicon bonded to both nitrogen and an organic material and having a  
7 dielectric constant no greater than 8.0 over said substrate; and

8           after forming the dielectric layer, exposing it to a plasma  
9 comprising nitrogen effective to reduce the dielectric constant to below  
10 what it was prior to said exposing.

11  
12           53. The method of claim 52 comprising exposing the dielectric  
13 layer to a plasma comprising nitrogen effective to reduce the dielectric  
14 constant to at least 15% below what it was prior to said exposing.

15  
16           54. The method of claim 52 wherein the nitrogen comprising  
17 plasma is at least in part derived from  $N_2$ .

18  
19           55. The method of claim 52 wherein the nitrogen comprising  
20 plasma is at least in part derived from  $NH_3$ .

21  
22           56. The method of claim 52 wherein the nitrogen comprising  
23 plasma is at least in part derived from  $N_2H_4$ .

24



1           57. The method of claim 52 wherein the nitrogen comprising  
2 plasma is at least in part derived from  $N_2O$ .

3  
4           58. The method of claim 52 wherein the nitrogen comprising  
5 plasma is at least in part derived from  $NO_x$ .

6  
7           59. The method of claim 52 wherein the exposing is void of  
8 oxygen.

9  
10          60. The method of claim 52 wherein the dielectric layer is  
11 formed by chemical vapor deposition in a chamber, the exposing  
12 occurring within the chamber without removing the substrate from the  
13 chamber between the forming and the exposing.

14  
15          61. The method of claim 52 wherein the plasma exposing is  
16 ineffective to appreciably etch the interlevel dielectric layer.

17  
18          62. The method of claim 52 wherein a whole of the dielectric  
19 layer subjected to the exposing is not transformed from one base  
20 chemistry to another by the exposing.

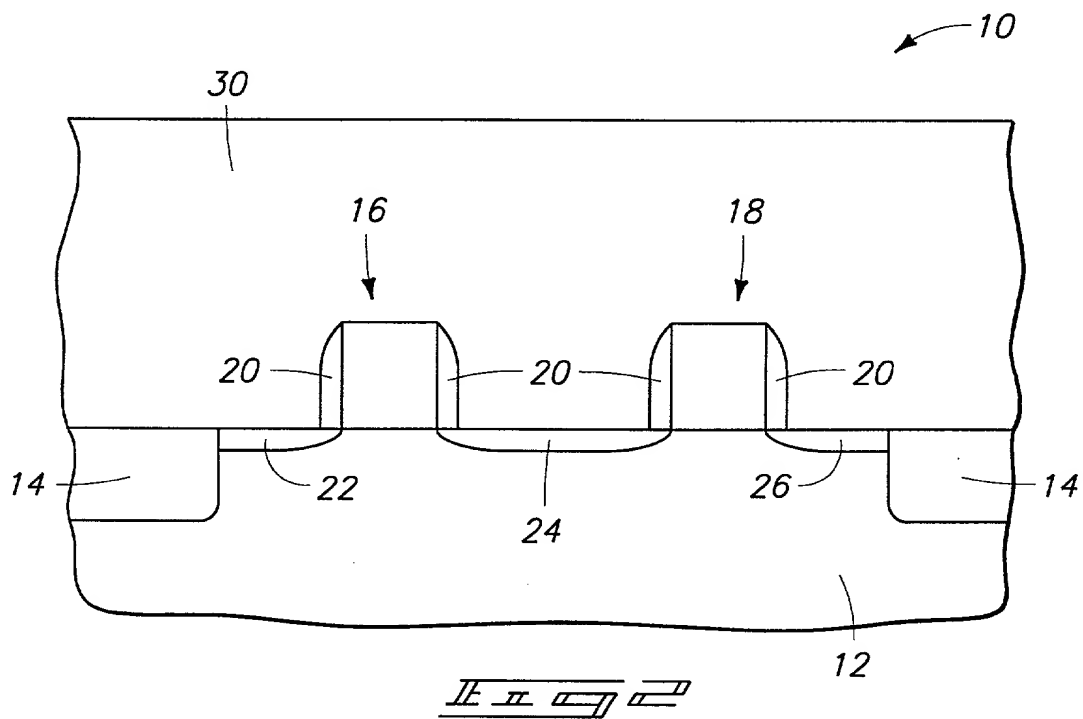
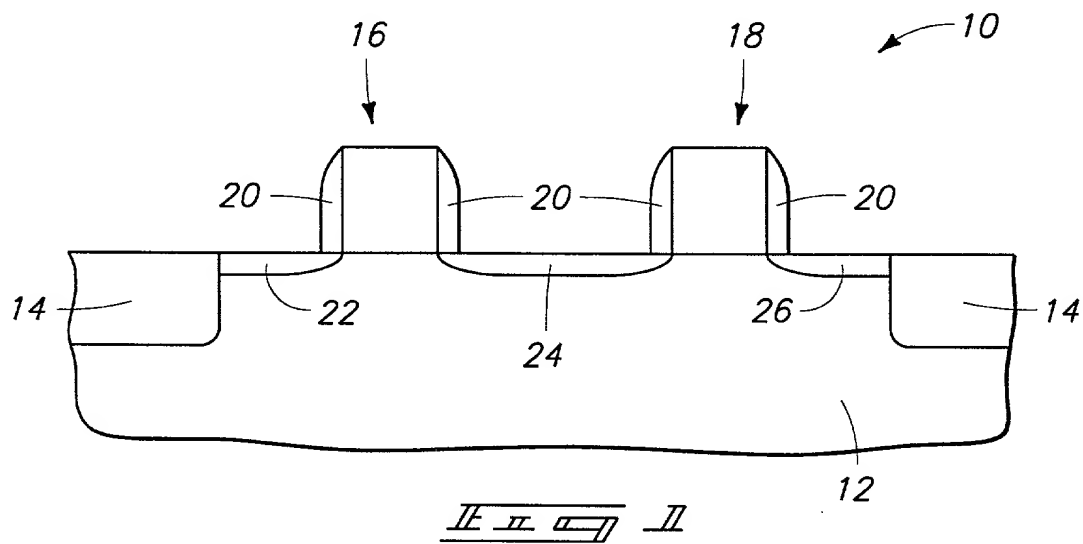
1           63. The method of claim 52 wherein the dielectric layer  
2 subjected to the exposing comprises  $(\text{CH}_3)_x\text{Si}_3\text{N}_{(4-x)}$ , with x being  
3 greater than 0 and no greater than 4.

4  
5           64. The method of claim 52 wherein the dielectric layer  
6 subjected to the exposing consists essentially of  $(\text{CH}_3)_x\text{Si}_3\text{N}_{(4-x)}$ , with  
7 x being greater than 0 and no greater than 4.  
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## ABSTRACT OF THE DISCLOSURE

A low k interlevel dielectric layer fabrication method includes providing a substrate having integrated circuitry at least partially formed thereon. An oxide comprising interlevel dielectric layer comprising carbon and having a dielectric constant no greater than 3.5 is formed over the substrate. After forming the carbon comprising dielectric layer, it is exposed to a plasma comprising oxygen effective to reduce the dielectric constant to below what it was prior to said exposing. A low k interlevel dielectric layer fabrication method includes providing a substrate having integrated circuitry at least partially formed thereon. In a chamber, an interlevel dielectric layer comprising carbon and having a dielectric constant no greater than 3.5 is plasma enhanced chemical vapor deposited over the substrate at subatmospheric pressure. After forming the carbon comprising dielectric layer, it is exposed to a plasma comprising oxygen at a subatmospheric pressure effective to reduce the dielectric constant by at least 10% below what it was prior to said exposing. The exposing occurs without removing the substrate from the chamber between the depositing and the exposing, and pressure within the chamber is maintained at subatmospheric between the depositing and the exposing.

1/1



DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Low k Interlevel Dielectric Layer Fabrication Methods, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

**PRIOR FOREIGN APPLICATIONS:**

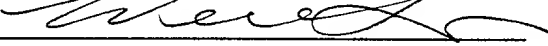
I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful

false statement may jeopardize the validity of the application or any patent issued therefrom.

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